SafeFLASH NAND Driver for Micron MT29FxG08 with ECC User Guide

Version 2.00

For use with SafeFLASH NAND Driver for Micron® MT29FxG08 with ECC versions 1.01 and above

Table of Contents

1. System Overview

This chapter contains the fundamental information for this module.

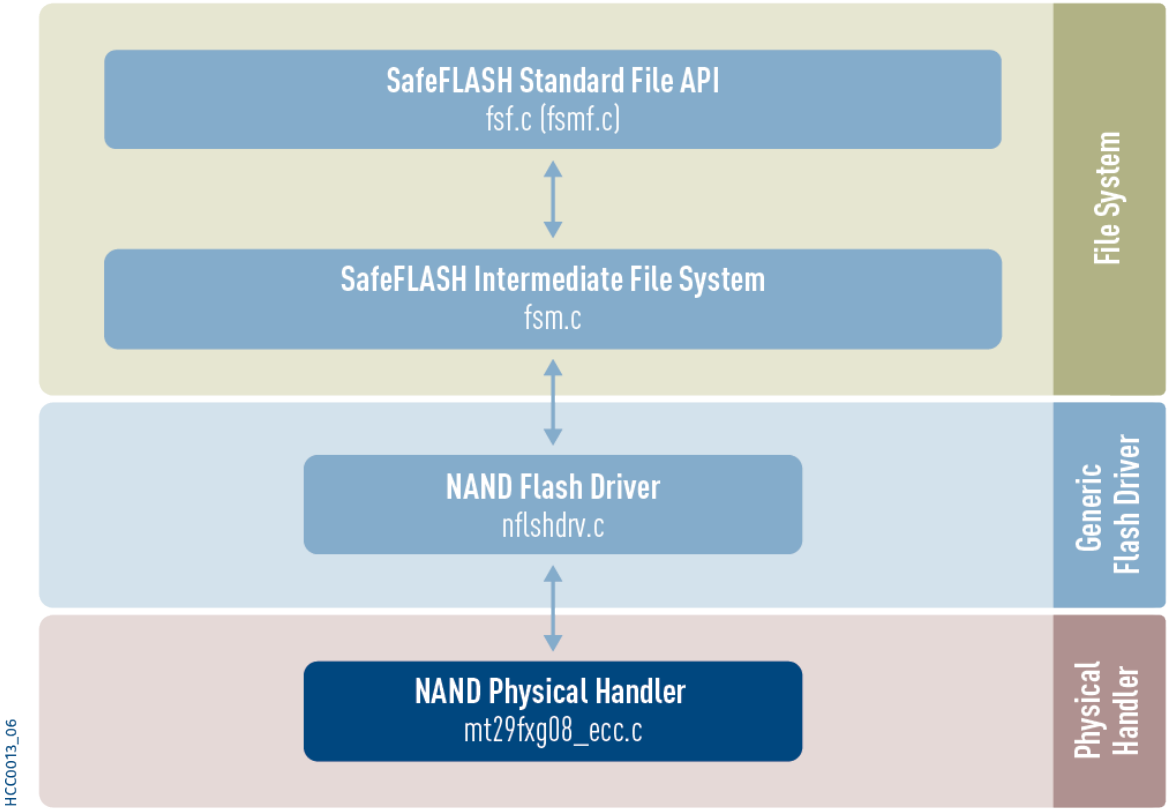
The component sections are as follows:

- Introduction – describes the main elements of the module.
- Feature Check – summarizes the main features of the module as bullet points.
- Device Description – summarizes the Micron devices supported.
- Fail-safety – defines fail-safety and describes the quality of service that SafeFLASH provides.
- Packages and Documents – the *Packages* section lists the packages that you need in order to use this module. The *Documents* section lists the relevant user guides.
- Change History – lists the earlier versions of this manual, giving the software version that each manual describes.

1.1. Introduction

This guide is for those who want to use HCC's NAND Media Driver for Micron® MT29FxG08 flash devices that use internal Error Correcting Code (ECC). The driver supports MT29F1G08, MT29F2G08, and MT29F4G08 devices that use internal ECC. This is for use with HCC's SafeFLASH file system.

The following diagram illustrates the structure of the file system software:



The main SafeFLASH package provides the file API and intermediate file system. This is described in the *HCC SafeFLASH File System User Guide*. This design is highly portable and gives excellent performance. The basic device architecture includes a high level driver for each general media type that shares some common properties. This driver handles issues of FAT maintenance, wear leveling, and so on.

The diagram also shows the following:

- The NAND Flash driver – the device driver for the NAND flash, provided by the base NAND package. This is described in the *HCC SafeFLASH File System NAND Drive User Guide*.
- The NAND physical handler – provided by this module, this performs the translation between the driver and the physical flash hardware.

Note: HCC Embedded offers hardware and firmware development consultancy to assist developers with the implementation of flash file systems.

1.2. Feature Check

The main features of the module are the following:

- Conforms to the HCC Advanced Embedded Framework.
- Designed for integration with both RTOS and non-RTOS based systems.
- Supports Micron® MT29FxG08 NAND flash drives that use internal Error Correcting Code (ECC) and is easily configurable for similar NAND flash parts.
- Supports static and dynamic wear leveling.
- Provides bad block management.

1.3. Device Description

This table summarizes the features of the supported devices.

Note: If internal ECC is not being used, consult sales@hcc-embedded.com about using a different HCC Micron® flash driver.

	MT29F1G08	MT29F2G08	MT29F4G08
Size (Gb)	1	2	4
Width	8	8	8
Plane size	2 planes x 512 blocks per plane	2 planes x 1024 blocks per plane	2 planes x 2048 blocks per plane
Page size	2048 bytes + 64 spare bytes.	2048 bytes + 64 spare bytes.	2048 bytes + 64 spare bytes.
Blocks	1024	2048	4096
Block size	64 pages (128K + 4K bytes)	64 pages (128K + 4K bytes)	64 pages (128K + 4K bytes)
Internal ECC	4 bit	4 bit	4 bit
SLC	Yes	Yes	Yes

1.4. Fail-safety

This driver for MT29FxG08 Serial NAND flash is designed as part of HCC's SafeFLASH file system. SafeFLASH guarantees a defined level of fail-safety (see the *SafeFLASH File System User Guide*). For the system to be able to guarantee fail-safety, each component must provide a defined quality of service.

For this driver the following must be guaranteed to ensure the system is fail-safe:

- All write operations must be committed to flash in the sequence in which they are provided to the driver.
- Any write operation that fails must return an error.
- Any erase operation that fails must return an error.
- The system must ensure that there is at most one partially complete write or erase operation. At this point the file system should be restarted so that it can be recovered.

To achieve this in practice, the target hardware should ensure that in the event of a falling voltage the system resets or signals when the level approaches the specified programming level of the flash chip and inhibits further flash access.

There are other ways to manage this, for instance by adding a capacitance to ensure power is still available to complete an operation after a hardware error or reset condition is detected.

By using these techniques, the system can guarantee correct operation even after an unexpected system reset.

1.5. Packages and Documents

Packages

The table below lists the packages that you need in order to use this module:

Package	Description
hcc_base_doc	This contains the two guides that will help you get started.
fs_safe_nand	The SafeFLASH NAND flash driver.
fs_safe_nand_drv_mt29fxg08_ecc	The SafeFLASH NAND driver for Micron MT29FxG08 with ECC package described in this document.

Documents

For an overview of HCC file systems and guidance on choosing a file system, see Product Information on the main HCC website.

Readers should note the points in the HCC Documentation Guidelines on the HCC documentation website.

HCC Firmware Quick Start Guide

This document describes how to install packages provided by HCC in the target development environment. Also follow the *Quick Start Guide* when HCC provides package updates.

HCC Source Tree Guide

This document describes the HCC source tree. It gives an overview of the system to make clear the logic behind its organization.

HCC SafeFLASH File System User Guide

This document describes the base SafeFLASH System.

HCC SafeFLASH File System NAND Drive User Guide

This document describes the SafeFLASH NAND driver that is used with the MT29FxG08 with ECC driver.

HCC SafeFLASH NAND Driver for Micron MT29FxG08 with ECC User Guide

This is this document.

1.6. Change History

To view or download manuals, see File System PDFs.

For the history of changes made to the package code itself, see History: fs_safe_nand_drv_mt29fxg08_ecc.

The current version of this manual is 2.00.

Manual version	Date	Software version	Reason for change
2.00	2020-02-03	1.01	New template.
1.00	2019-01-23	1.01	First online version.

2. Source File List

The following sections describe all the source code files included in the system. These files follow the HCC Embedded standard source tree system, described in the *HCC Source Tree Guide*. All references to file pathnames refer to locations within this standard source tree, not within the package you initially receive.

Note: Do not modify any files except the configuration file and PSP files.

Configuration File

The file **src/config/config_safe_nand_mt29fxg08_ecc.h** contains the configurable parameters of the system. Configure these as required. This is the only file in the module that you should modify. For details of the options, see Configuration Options.

System Files

These files are in the directory **src/safe-flash/nand/phy/micron**. **These files should only be modified by HCC**.

File	Description
mt29fxg08_ecc.c	Driver source code.
mt29fxg08_ecc.h	Driver header file.

Version File

The file **src/version/ver_safe_nand_mt29fxg08_ecc.h** contains the version number of this module. This version number is checked by all modules that use this module to ensure system consistency over upgrades.

Platform Support Package (PSP) Files

These files in the directory **src/psp/target/safe_nand_mt29fxg08_ecc** provide the functions. Modify these files as required for your hardware; see PSP Porting.

Note:

- These are PSP implementations for the specific microcontroller and board; you may need to modify these to work with a different microcontroller and/or development board.
- In the package these files are offset to avoid overwriting an existing implementation. Copy them to the root **hcc** directory for use.

The files are as follows:

File	Description
psp_nand_mt29fxg08_ecc.c	Low level initialization function source.
psp_nand_mt29fxg08_ecc.h	Header file.

The PSP also has a version file, **ver_psp_nand_mt29fxg08_ecc.h**.

3. Configuration Options

Set the system configuration options in the file **src/config/config_safe_nand_mt29fxg08_ecc.h**. This section lists the available options and their default values.

S_MT29FXG08_ECC_ID

The NAND ID for MT29F4G08ABADA. The default is:

```
( ( 0x2C << 0 ) | ( 0xDC << 8 ) | ( 0x90 << 16 ) | ( 0x95 << 24 ) )
```

S_MT29FXG08_BLOCK_START

Set this to the number of blocks at the start to preserve for custom use. The default is 128 blocks.

S_MT29FXG08_BLOCK_END

The final block. The default is 4095.

S_MT29FXG08_SECTOR_SIZE

The sector size. The default is 0x4000; this is 16K - calculated by the **FSmem.exe** utility as suitable for the MT29F4G08.

S_MT29FXG08_SEPARATE_DIR

Keep the default of 1 to place a directory in a separate block. Otherwise, set this to 0.

4. PSP Porting

The Platform Support Package (PSP) is designed to hold all platform-specific functionality, either because it relies on specific features of a target system, or because this provides the most efficient or flexible solution for the developer.

The files **psp_nand_mt29fxg08_ecc.c** and **psp_nand_mt29fxg08_ecc.h** define the functions, which are described in the following sections. Modify these files as required for your hardware.

Function	Description
psp_nand_mt29fxg08_ecc_init()	Initializes the hardware.
psp_nand_mt29fxg08_ecc_wait_ready()	Specifies the maximum number of ticks to wait for R/B# to become asserted.

4.1. psp_nand_mt29fxg08_ecc_init

Use this function to initialize the hardware. This configures pins and clocks. It is called from the mlayer lowinit function once.

Format

```
uint32_t psp_nand_mt29fxg08_ecc_init ( void )
```

Arguments

None.

Return Values

Return value	Description
0	Successful execution.
Else	Operation failed.

4.2. psp_nand_mt29fxg08_ecc_wait_ready

Use this function to specify the maximum number of ticks to wait for R/B# to become asserted.

Format

```
uint32_t psp_nand_mt29fxg08_ecc_wait_ready ( uint32_t tick )
```

Arguments

Argument	Description	Type
tick	The maximum number of ticks to wait.	uint32_t

Return Values

Return value	Description
0	R/B# was asserted.
1	R/B# was not asserted.

5. Version

Version 2.00

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