SafeFLASH NOR Driver for CFI and SFDP SPI Flash User Guide

Version 1.20

For use with SafeFLASH NOR Driver for CFI and SFDP SPI Flash versions 1.09 and above

Date: 31-Aug-2017 15:25

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1 System Overview

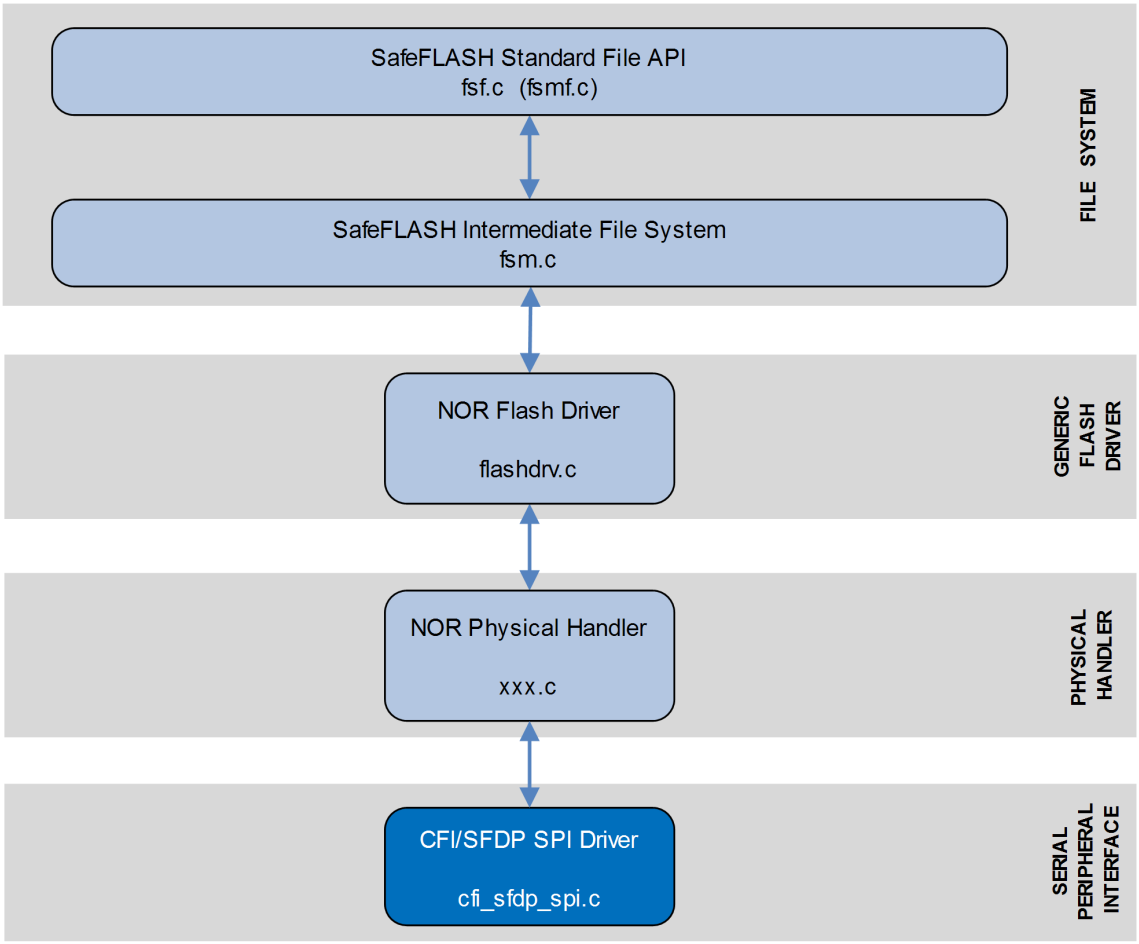
1.1 Introduction

This guide is for those who want to implement a SafeFLASH NOR driver for use with CFI/SFDP SPI flash devices. This is for use with HCC's SafeFLASH file system. These flash devices support the Common Flash Memory Interface (CFI) and Serial Flash Discoverable Parameters (SFDP) standards on a Serial Peripheral Interface (SPI).

CFI and SFDP are standards widely used by flash manufacturers that allow software to obtain detailed information about the internal configuration of the flash device. This driver uses that information to configure the system automatically to use the attached flash type.

The SafeFLASH file system driver design is highly portable while still maintaining excellent performance. The basic device architecture includes a high level driver for each general media type that shares some common properties. This driver handles issues of FAT maintenance, wear leveling, and so on.

The following diagram shows the structure of the file system software:



This diagram shows:

- The main SafeFLASH package – this provides the file API and intermediate file system. This is described in the *HCC SafeFLASH File System User Guide*.
- The NOR flash driver – the generic device driver for NOR flash, provided by the base NOR package. This driver handles issues of FAT maintenance, wear leveling, and so on. It is described in the *HCC SafeFLASH File System NOR Drive User Guide*.
- The NOR physical handler – provided by this module, this performs the translation between the driver and the physical flash hardware.
- The CFI/SFDP SPI driver – the NOR device driver for the CFI/SFDP SPI flash. This guide shows how to add this to the build. Using the available sample drivers as a model, you can create a driver that meets your specific needs.

Note: HCC Embedded offers hardware and firmware development consultancy to assist developers with the implementation of flash file systems.

1.2 Feature Check

The main features of the module are the following:

- Conforms to the HCC Advanced Embedded Framework.
- Designed for integration with both RTOS and non-RTOS based systems.
- Supports NOR flash connected by SPI.
- Supports all common NOR devices.
- Can handle any array of NOR flash.
- Supports the Common Flash Memory Interface (CFI) standard for NOR flash devices.
- Supports the Serial Flash Discoverable Parameters (SFDP) standard for serial NOR flash devices.

1.3 Fail-safety

This driver for serial NOR flash is designed as part of HCC's SafeFLASH file system. SafeFLASH guarantees a defined level of fail-safety (see the *SafeFLASH File System User Guide*). For the system to be able to guarantee fail-safety, each component must provide a defined quality of service.

For this driver the following must be guaranteed to ensure the system is fail-safe:

- All write operations must be committed to flash in the sequence in which they are provided to the driver.
- Any write operation that fails must return an error.
- Any erase operation that fails must return an error.
- The system must ensure that there is at most one partially complete write or erase operation. At this point the file system should be restarted so that it can be recovered.

To achieve this in practice, the target hardware should ensure that in the event of a falling voltage the system resets or signals when the level approaches the specified programming level of the flash chip and inhibits further flash access.

There are other ways to manage this, for instance by adding a capacitance to ensure power is still available to complete an operation after a hardware error or reset condition is detected.

By using these techniques, the system can guarantee correct operation even after an unexpected system reset.

1.4 Packages and Documents

Packages

The table below lists the packages that you need in order to use this module:

Package	Description
hcc_base_doc	This contains the two guides that will help you get started.
fs_safe_nor	The SafeFLASH NOR flash driver.
fs_safe_nor_drv_cfi_sfdp_spi	The NOR driver for CFI and SFDP package described in this document.
psp_template_spi	The SPI Platform Support Package (PSP).

Documents

For an overview of HCC file systems and guidance on choosing a file system, see Product Information on the main HCC website.

Readers should note the points in the HCC Documentation Guidelines on the HCC documentation website.

HCC Firmware Quick Start Guide

This document describes how to install packages provided by HCC in the target development environment. Also follow the *Quick Start Guide* when HCC provides package updates.

HCC Source Tree Guide

This document describes the HCC source tree. It gives an overview of the system to make clear the logic behind its organization.

HCC SafeFLASH File System User Guide

This document describes the base SafeFLASH System.

HCC SafeFLASH File System NOR Drive User Guide

This document describes the SafeFLASH NOR driver that is used with the NOR CFI/SFDP SPI package.

HCC SafeFLASH NOR Driver for CFI and SFDP SPI Flash User Guide

This is this document.

1.5 Change History

This section describes past changes to this manual.

- To view or download earlier manuals, see Archive: SafeFLASH NOR Driver for CFI-SFDP SPI Flash User Guide.
- For the history of changes made to the package code, see History: fs_safe_nor_drv_cfi_sfdp_spi.

The current version of this manual is 1.20. The full list of versions is as follows:

Manual version	Date	Software version	Reason for change
1.20	2017-08-31	1.09	Corrected *Packages* list.
1.10	2017-06-26	1.08	New *Change History* format.
1.00	2017-04-24	1.08	First online version.

2 Source File List

The following sections describe all the source code files included in the system. These files follow the HCC Embedded standard source tree system, described in the *HCC Source Tree Guide*. All references to file pathnames refer to locations within this standard source tree, not within the package you initially receive.

> **Note:** Do not modify any files except the configuration file and PSP files.

2.1 Configuration File

The file **src/config/config_safe_nor_cfi_sfdp.h** contains the configurable parameters of the system. Configure these as required. For detailed explanation of these options, see Configuration Options.

2.2 System Files

These files are in the directory **src/safe-flash/nor/phy/cfi_sfdp**. **These files should only be modified by HCC.**

File	Description
cfi_sfdp_spi.c	SPI driver source code.
cfi_sfdp_spi.h	SPI driver header file.

2.3 Platform Support Package (PSP) Files

These files in the directory **src/psp/target/safe_nor_cfi_sfdp** define the psp_safe_nor_cfi_sfdp_delay() function. Modify these files as required for your hardware.

File	Description
psp_safe_cfi_sfdp.c	Source code defining the **psp_safe_nor_cfi_sfdp_delay()** function. This waits at least 100 ns, the chip-select deselect time.
psp_safe_cfi_sfdp.h	Header file.

2.4 Version File

The file **src/version/ver_safe_nor_cfi_sfdp.h** contains the version number of this module. This version number is checked by all modules that use this module to ensure system consistency over upgrades.

3 Configuration Options

Set the configuration options in the file **src/config/config_safe_nor_cfi_sfdp.h**. This section lists the available configuration options and their default values.

NOR_PAGE_SIZE

The maximum number of bytes for the page program command. The default is 256.

NOR_BLOCK_THRESHOLD

The block sector size threshold. Below this number of blocks, a 4K sector size is preferred. The default is 128.

> **Note:** Set the following four parameters according to the type of flash used.

NOR_BLOCKSTART

Specify the space before the block start that is not to be used by the file system. The default is 0.

NOR_SECTORSIZE

The logical sector size. This must be less than or equal to the block size (*g_block_size*/NOR_BLOCK_SIZE or NOR_VIRTUAL_BLOCK_SIZE). The default is 512.

NOR_DESCSIZE

The descriptor size. This must be less than or equal to the block size (*g_block_size*/NOR_BLOCK_SIZE or NOR_VIRTUAL_BLOCK_SIZE). The default is 16384.

NOR_CACHEDESCSIZE

The cache size. This must be less than the descriptor size (NOR_DESCSIZE). The default is 2048.

NOR_VIRTUAL_BLOCK_SIZE

Physical blocks can be joined to a larger virtual block (to allow use of a larger descriptor block). Set this option to 0 to disable virtual blocks, otherwise it is must be a multiple of g_block_size/NOR_BLOCK_SIZE. The default is 16384.

> **Note:** The following three parameters are only used if flash identification is not possible using SFDP nor CFI.

NOR_BLOCK_SIZE

The block size. The default is 4096.

NOR_NUM_BLOCKS

The number of blocks. The default is 128.

NOR_CMD_ERASE

The erase command for the block size specified by NOR_BLOCK_SIZE. The default is 0x20.

NOR_TBPARM_TOP

If this is non-zero, the driver checks whether the TBPARM bit is set (that is, whether the device is already configured to have parameter sectors on the top of the address space). If this OTP bit is not set, it sets it. The default is 1.

NOR_SPI_UNIT

The SPI ID to use. The default is 0.

NOR_SPI_BAUDRATE

The SPI clock frequency in Hz . The default is 20000000.

NOR_TMO_ERASE_MS

The erase timeout in milliseconds. The default is 3000.

NOR_TMO_PROGRAM_MS

The program timeout in milliseconds. The default is 500.

NOR_TMO_WREN_MS

The write enable timeout in milliseconds. The default is 5.

NOR_TMO_WRITE_SR_MS

The write status register timeout in milliseconds. The default is 8.

4 PSP Porting

The Platform Support Package (PSP) is designed to hold all platform-specific functionality, either because it relies on specific features of a target system, or because this provides the most efficient or flexible solution for the developer.

The files **psp_safe_cfi_sfdp.c** and **psp_safe_cfi_sfdp.h** define the psp_safe_nor_cfi_sfdp_delay() function. Modify these files as required for your hardware.

4.1 psp_safe_nor_cfi_sfdp_delay

Use this function to wait for at least 100 ns, which is the chip select/deselect time.

Format

```
void psp_safe_nor_cfi_sfdp_delay ( void )
```

Arguments

None.

Return Values

None.